WHAT IS CLAIMED IS:

1. A processor comprising:

an execution circuit configured to execute an instruction, the execution circuit including at least a first subcircuit and a second subcircuit;

an issue circuit coupled to the execution circuit, wherein the issue circuit is configured to issue an instruction to the execution circuit, and wherein the issue circuit is configured to generate a control signal responsive to whether or not the instruction is issued to the execution circuit; and

a clock tree for clocking circuitry in the processor, wherein a portion of the clock tree supplies a plurality of clocks to the execution circuit, the plurality of clocks including at least a first clock clocking the first subcircuit and at least a second clock clocking the second subcircuit, the portion of the clock tree coupled to receive the control signal for collectively conditionally gating the plurality of clocks, and wherein the portion of the clock tree is configured to individually conditionally gate at least some of the plurality of clocks responsive to activity in the respective subcircuits of the execution circuit.

2. The processor as recited in claim 1 wherein the issue circuit is configured to generate the control signal in a state not gating the plurality of clocks for a plurality of consecutive clock cycles in response to issuing the instruction.

3. The processor as recited in claim 2 wherein the clock tree is configured to individually gate the plurality of clocks on a clock cycle by clock cycle basis.

4. The processor as recited in claim 3 wherein the issue circuit includes a counter corresponding to the execution circuit, and wherein the issue circuit is configured to initialize the counter responsive to issue of the instruction.

5. The processor as recited in claim 4 wherein the issue circuit is configured to reinitialize the counter responsive to issuing a second instruction to the execution circuit.

6. The processor as recited in claim 4 wherein the issue circuit is configured to decrement the counter each clock cycle, and wherein the issue circuit is configured to continue generating the control signal in the state not gating the plurality of clocks responsive to the counter having a non-zero value.

7. The processor as recited in claim 4 wherein the issue circuit is configured to initialize the counter based on a latency of the execution circuit in executing the instruction.

8. The processor as recited in claim 7 wherein the counter is initialized to a number of clock cycles greater than or equal to the latency.

9. The processor as recited in claim 8 wherein the counter is initialized to a number of clock cycles equal to the latency.

10. The processor as recited in claim 1 wherein the execution circuit comprises a floating point unit.

11. The processor as recited in claim 10 wherein the first subcircuit comprises an adder circuit and wherein the second subcircuit comprises a multiplier circuit.

12. The processor as recited in claim 11 further comprising a third subcircuit clocked by at least a third clock of the plurality of clocks, wherein the third subcircuit includes an

approximation circuit.

13. The processor as recited in claim 1 wherein the execution circuit comprises circuitry for executing a load/store instruction.

14. The processor as recited in claim 1 wherein the first subcircuit comprises a load/store unit and wherein the second subcircuit comprises a data cache.

15. An apparatus comprising:

a first circuit including at least a first subcircuit and a second subcircuit; and

a clock tree having a clock input, a control input, and a plurality of clock outputs, at least a first clock output of the plurality of clock outputs coupled to the first subcircuit and at least a second clock output of the plurality of clock outputs coupled to the second subcircuit;

wherein the plurality of clock outputs are collectively conditionally gated from the clock input responsive to the control input; and

wherein at least some of the plurality of clock outputs are individually conditionally gated from the clock input further responsive to circuitry monitoring activity in the respective subcircuits.

16. The apparatus as recited in claim 15 further comprising a second circuit coupled to the control input, the second circuit configured to generate the control input, and wherein the second circuit is configured to generate the control input in a state to not gate for a plurality of consecutive clock cycles responsive to an event, and wherein the circuitry monitoring activity operates on a clock cycle by clock cycle basis.

17. The apparatus as recited in claim 15 wherein the clock tree comprises a plurality of levels of clock buffer circuitry, and wherein a first level of the plurality of levels includes one or more logic gates which combine the clock input and the control input.

18. The apparatus as recited in claim 17 wherein a number of the plurality of levels is 4.

19. The apparatus as recited in claim 15 further comprising:

a second circuit including at least a third subcircuit and a fourth subcircuit; and

a second clock tree having a second clock input, a second control input, and a second plurality of clock outputs, at least a third clock output of the second plurality of clock outputs coupled to the third subcircuit and at least a fourth clock output of the second plurality of clock outputs coupled to the fourth subcircuit;

wherein the second plurality of clock outputs are collectively conditionally gated from the second clock input responsive to the second control input; and

wherein at least some of the second plurality of clock outputs are individually conditionally gated from the second clock input further responsive to circuitry monitoring activity in the respective subcircuits.

20. A carrier medium comprising one or more data structures representing:

a first circuit including at least a first subcircuit and a second subcircuit; and

a clock tree having a clock input, a control input, and a plurality of clock outputs,

at least a first clock output of the plurality of clock outputs coupled to the first subcircuit and at least a second clock output of the plurality of clock outputs coupled to the second subcircuit;

wherein the plurality of clock outputs are collectively conditionally gated from the clock input responsive to the control input; and

wherein at least some of the plurality of clock outputs are individually conditionally gated from the clock input further responsive to circuitry monitoring activity in the respective subcircuits.